Taskbook - 2021
Communication Systems and Protocols

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Task 1: Data transmission

The Compact Muon Solenoid (CMS) experiment is one of two large general-purpose particle physics detectors built on the Large Hadron Collider (LHC) at CERN in Switzerland and France. On one single day the experiment produces about 20 TB (Terabyte = $1*10^{12}$ bytes) of interesting data. These data has to be transferred to GridKa (Karlsruhe, approx. 450 km distance). The following transport schemes are available:

(i) Transmission over VDSL (50 Mbit/s)
(ii) Transmission over an optical fiber link (110Gbit/s)
(iii) Transport of the data using a hard disk and a car (95 km/h)

A) Calculate the time required to transfer the data using the different options. Hint: Use 1 Kbit = 1000 bit for the calculation.

Task 2: Reflection on wires

A setup consisting of a voltage source with an internal resistance $R_I = 50\Omega$ as sender and a receiver with $R_T = 175\Omega$ is shown in Figure 2. The DC resistance of the line is zero, the characteristic impedance Z_0 is 75Ω.

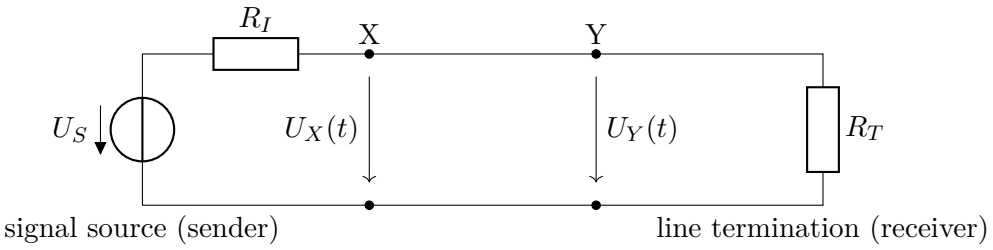


Figure 2.1: Test setup

At the time t= 0 the voltage U_s of the sender changes from $0V$ to $5V$ and is constant afterwards. The run time of a wave on the wire is t_d.

A) What is the value of the voltage at point X at the time $t = 0$?

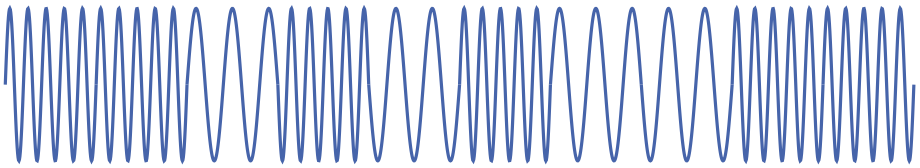
B) Which voltage value appears at the points X and Y after an infinite amount of time?

C) Calculate the voltages at the points X and Y at the times $t = 0 \ldots 5t_d$. Neglect all transient events, use ideal rectangular impulses for calculation.

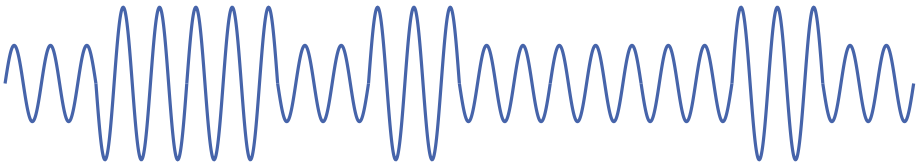
Task 3: Modulation

Give the type of modulation used for the signals as shown in the diagram below. Give also the data that is being transmitted. Assume a constant bit length.

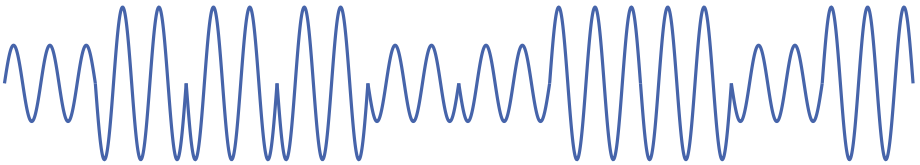
A)



B)



C)



Task 4: Line Codes

A) Draw the digital signals for the bit string 101 100 000 011 using each of the NRZ, RZ, NRZI-S, AMI and differential Manchester digital encoding schemes. Use Figure 4.1.

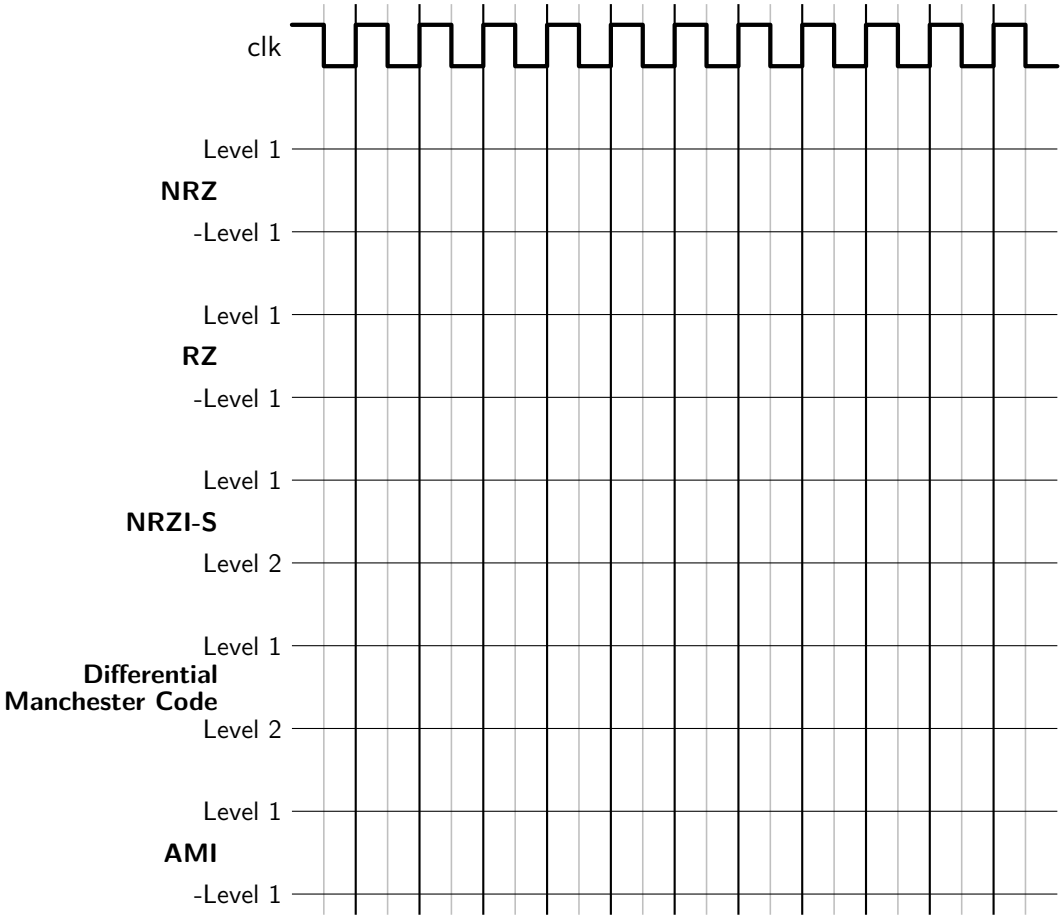


Figure 4.1: Line codes

B) Encode the following bit string using the 4B/5B code:

101000001111111000010111

C) What is the longest sequence of "0" if the 4B/5B code is used?

D) What is the longest sequence of "1" if the 4B/5B code is used?

E) Figure 4.2 shows the signal sequence for a Manchester II coded signal. Determine the associated bit string.

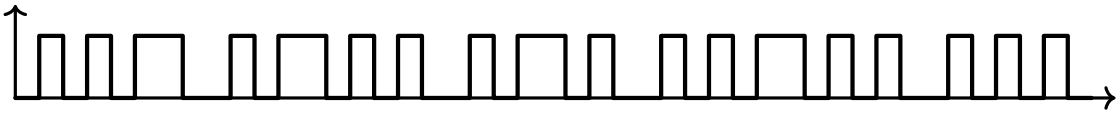


Figure 4.2: Manchester II coded bit string

Task 5: Physical Basics

Task 5.1: TTL-Logic

A) Insert the logic level (HIGH, LOW) of the output and the state of the transistors (conducts, blocks) into the table 5.1 according to the input configuration x_1 and x_2 at the standard TTL output driver in figure 5.1.

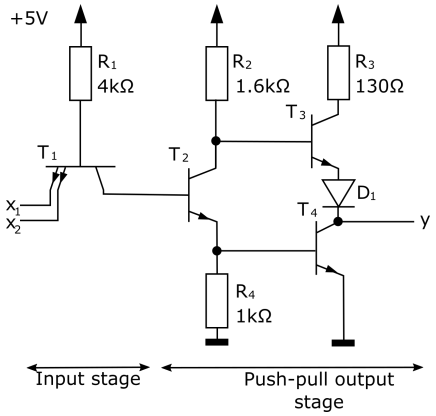


Figure 5.1: standard TTL output driver

x_1	x_2	T_1	T_2	T_3	T_4	y
0	0					
0	1					
1	0					
1	1					

Table 5.1: Logic Level

B) List two advantages when using TTL drivers.

C) How would it be possible to overcome the disadvantage of possible short circuits of a TTL driver? Which part of the TTL driver needs to be modified? Modify the Figure 5.2 to get the solution and describe the purpose of te adjustments made.

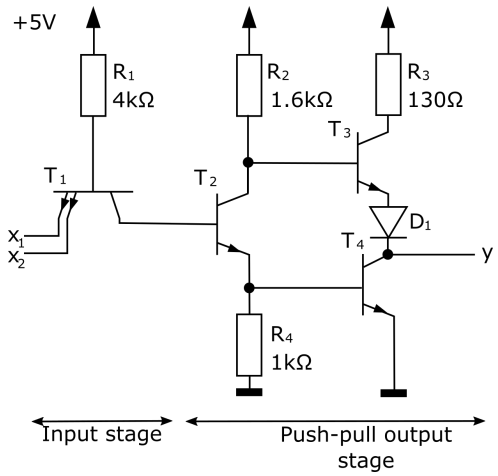


Figure 5.2: TTL driver

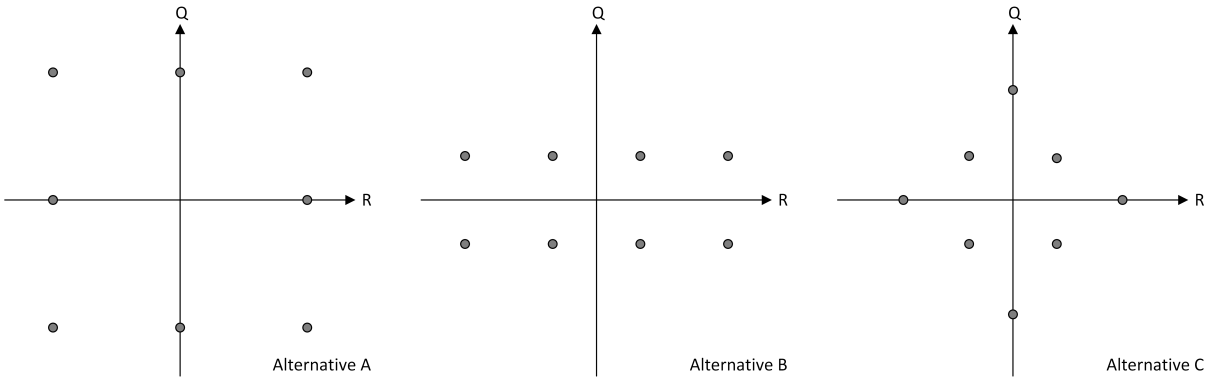
Task 5.2: Differential Signals

A) How could differential signal generation be realized?

B) What are the advantages for differential signal transmission? Name two.

Task 5.3: Modulation

Now consider the following constellation diagrams for 8-QAM. All diagrams are drawn with the same scaling of the axes.



A) If you had to realize a communication system using QAM modulation, which alternative would you choose? Give reasons for your decision

B) Briefly describe PSK modulation and give one advantage.

Task 5.4: Channel capacity, Bandwidth

A digital transmission system with a bandwidth of $B = 1,5 * 10^6 Hz$ has a channel capacity of $C = 5Mbit/s$ (according to Shannon).

A) What is the minimum for the signal to noise ratio (SNR) in dB?

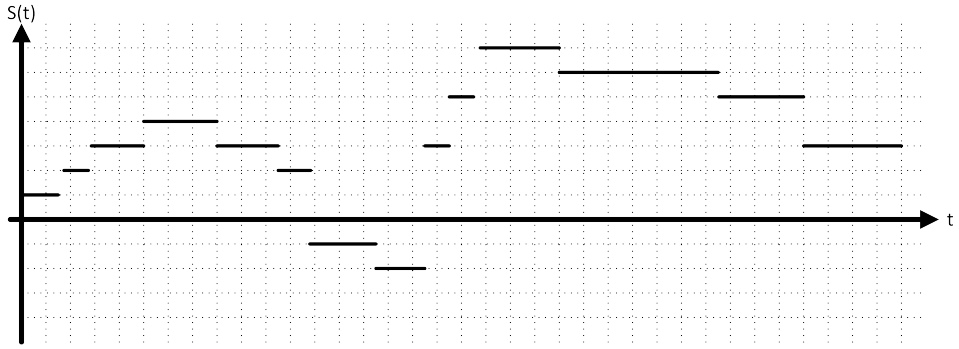
B) Give the definition for the Cut-Off-Frequency:

Task 5.5: Signal Conversion

A) When converting analog signals into digital signals, what has to be considered in order to be able to achieve an unambiguous reconstruction of the signal (name and formula)?

B) One can distinguish four different classes of signal. What are the parameters that are changed to form these classes? Give the combination of parameters that are characteristic for each class.

C) Which signal class does the following signal belong to? Briefly describe where this type of signal can be used.



Task 6: Wiring

Task 6.1: General Questions

A) What is a symmetric line? Name one disadvantage of symmetric signaling.

B) How does the wire length affect the characteristic impedance Z_W in a lossless case?

C) Name four causes for distortions of real data signals.

D) Name the four different possible cases of the reflection factor r and describe shortly their mechanical analogue.

Task 6.2: Reflection on wires

You have found a transmission link in the basement and want to find out the characteristic impedance. With the setup given in Figure 6.2 you make the measurements that can be seen in Figure 6.2. The signal source U_S is stuck at an unknown output voltage and has an internal resistance of 33Ω. The termination resistance is $R_T = 200\Omega$. You can assume that the DC resistance is zero. When using numbers from Figure 6.2, only use one decimal place and only use values where the voltage is mostly constant.

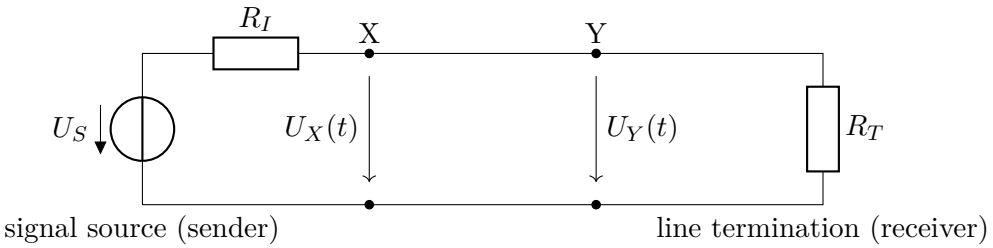


Figure 6.1: Test setup

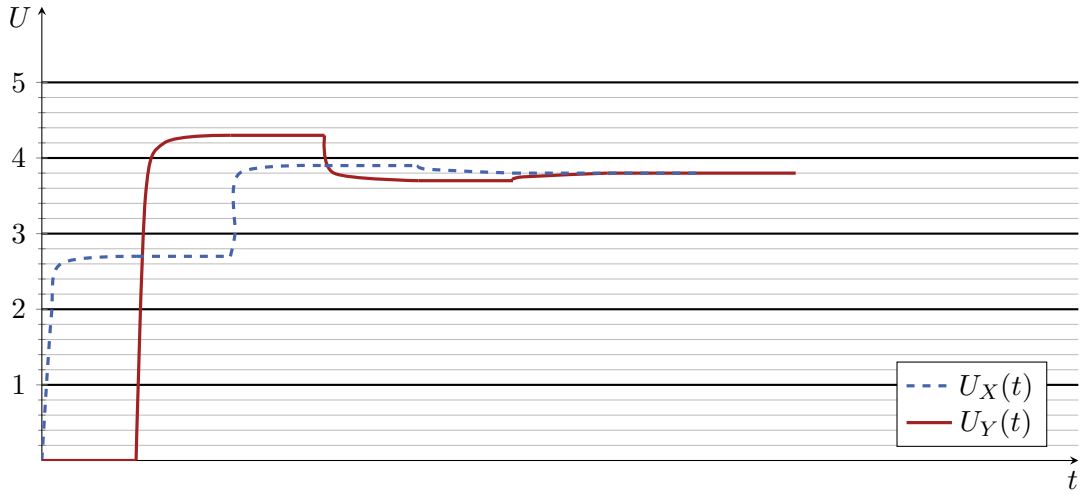


Figure 6.2: Measurement

A) How would you divide the timeline? Explain and mark at least four points on the timeline

B) Without calculation, make a quantitative statement about the reflection factors at the start and at the end.

C) Calculate the characteristic impedance Z_0 and the reflection factors at the start and at the end.

D) Calculate the internal sender voltage U_s

Task 7: Data Transmission

Task 7.1: Line Codes

A) Draw the digital signals for the bit string 010 101 111 000 011 using each of the NRZ, Manchester II, and differential Manchester digital encoding schemes. Use figure 7.1.

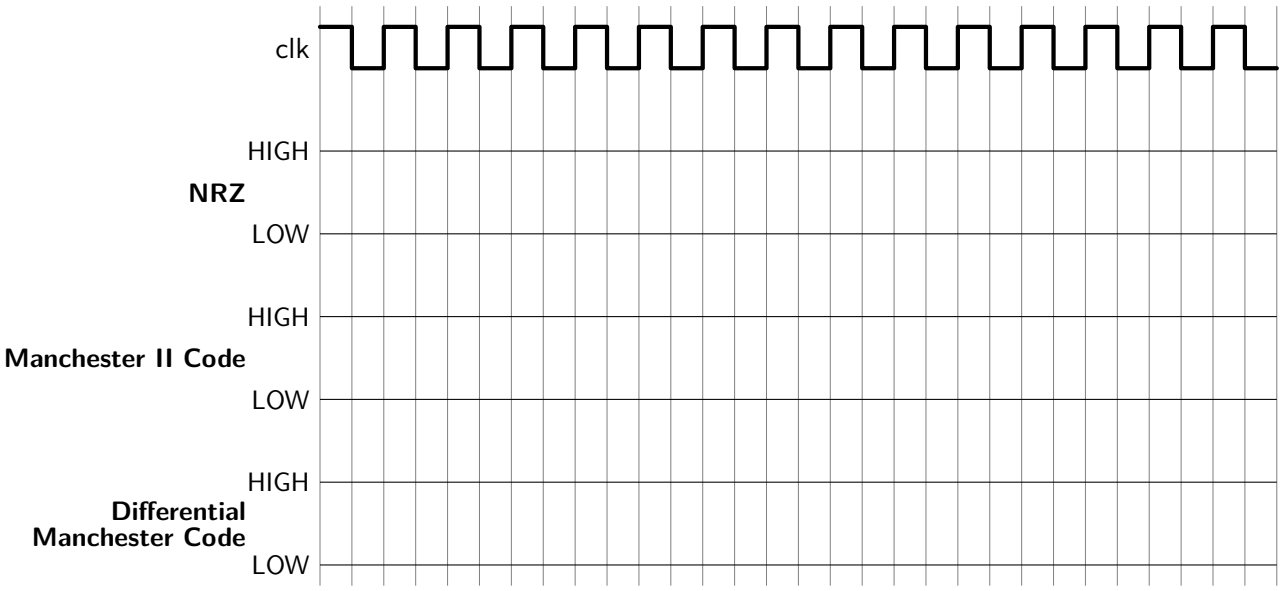


Figure 7.1: Line codes

Task 7.2: CDMA

A) What are the requirements for spreading codes used by CDMA?

Sender node	Function
A	$(+1, +1, -1, -1, +1, +1, -1, -1)$
B	$(+1, +1, +1, +1, -1, +1, -1, +1)$
C	$(+1, +1, -1, -1, -1, -1, +1, +1)$

Table 7.1: Functions for sender nodes

B) Table 7.1 shows the functions of several sender nodes. Show that these functions fulfill the requirements and can be used to transmit data using CDMA.

C) An additional node D should also be able to send data at the same time. Find another function for node D and show that your function is valid.

Task 7.3: Symbol Stuffing

You want to transmit formatted text but due to limitations of your transmission system you can only use the uppercase letters A-Z and whitespace. However, it should be possible to transmit italic, bold and strike-through text.
To achieve this, the command character “C” is used which denotes the beginning and the end of a command sequence. The commands are then applied to all following characters until the command sequence is repeated. If the character “C” is to be sent as part of the text, it therefore has to be escaped by doubling it at sender site. Available commands are “B” for bold text, “I” for italic text, “L” for lowercase letters and “S” for strike-through text.

A) Format the following text according to these rules:

This task is ~~**stupid**~~ *COOL*

B) What could happen if you did not use commands with an additional separating command word?

Task 8: Code Division Multiple Access (CDMA)

A) The transmission scheme “Code Division Multiple Access” uses so called spreading codes to separate different transmissions. One group of functions that can be used for this purpose, are the Walsh functions. The CDMA scheme shall be used for simultaneous transmission of eight different messages. Derive the required Walsh functions.

B) For the simultaneous transmission of three messages, the Walsh function calculated in this task shall be used. The eight bit given in Table 8.1 shall be encoded each using one of the Walsh functions mentioned above. They are the transmitted simultaneously. The Walsh function is to be inverted when a ‘0’ is to be transmitted and remains unchanged for a ‘1’ to be send. Give the resulting signal on the media. Make use of the given scheme.

Node	Data	Signal							
0	"0"								
3	"1"								
6	"0"								
Signal on media									

Table 8.1: transmission with CDMA

C) The following Signal has been received from a transmission using the Walsh functions from this task.

+2.1 +1.9 +1.4 +2.0 -1.7 +5.3 -2.1 -1.9

As corruptions might happen during transmission, the receiver has a tolerance band for the detection of "1" and "0". All values differing up to ±0.5 from the ideal value will still be accepted as "1" and "0". Calculate the bit value that the receiver will detect for node 1 and node 5.

Task 9: Carrier Sense Multiple Access/Collision Detection (CSMA/CD)

In this task we have a look at a bus system with arbitration that is derived from CSMA/CD. The following rules apply:

- All nodes want to send as many messages as possible. The length of each message is given in Table 9.1.
- A node is not allowed to send twice in a row. After each successful transmission it has to wait until another node has finished its transmission. The values of the assigned waiting times for each node are given in Table 9.1.
- If a node willing to send detects that the bus is occupied it withdraws and waits for the time specified in Table 9.1 (waiting time) until it will retry to transmit. Any ongoing transmission is not influenced.
- If two or more nodes want to start a transmission on the free bus at the same time there is a collision. All involved nodes withdraw from the bus and wait for the time given in Table 9.1. If a node was already waiting before, its waiting time will be doubled. The waiting time is only reset to the initial value after a successful transmission of the respective node.

Node	Packet length	Waiting time
A	2	1
B	2	2
C	2	3

Table 9.1: Specification of nodes

A) Fill in the signal sequence of the bus nodes, resulting from the specification as given above (use Figure 9.1). Mark waiting times and collisions that occur.

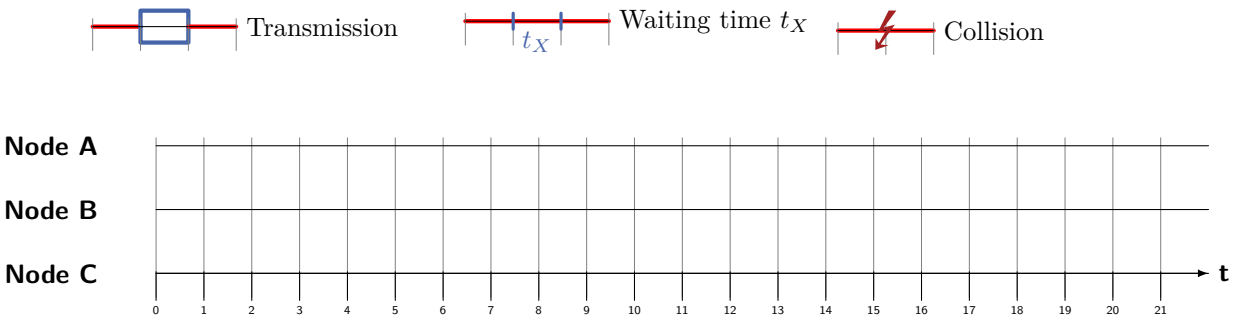


Figure 9.1: Signal sequence

Task 10: Media Access

Task 10.1: CSMA/CD

In this task we have a look at a bus system with arbitration that is derived from CSMA/CD. The following rules apply:

- All nodes want to send as many messages as possible. The length of each message is given in table 10.1
- A node is not allowed to send twice in a row. After each successful transmission it has to wait until another node has finished its transmission. The values of the assigned waiting times for each node are given in table 10.1.
- If a node willing to send detects that the bus is occupied it withdraws and waits for the time specified in table 10.1 (waiting time) until it will retry to transmit. Any ongoing transmission is not influenced.
- If two or more nodes want to start a transmission on the free bus at the same time there is a collision. All involved nodes withdraw from the bus and wait for the time given in table 10.1.

Node	Packet length	Waiting time
A	1	2
B	2	2
C	3	2

Table 10.1: Specification of nodes

A) Fill in the signal sequence of the bus nodes, resulting from the specification as given above (use Figure 10.1). Mark waiting times and collisions that occur.

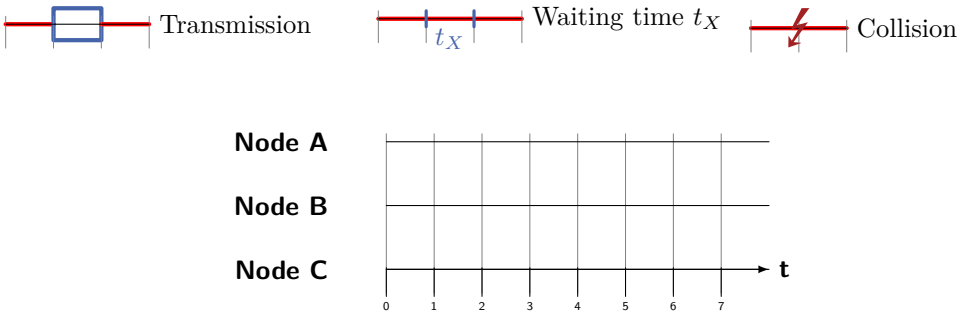
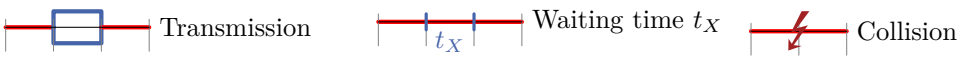


Figure 10.1: Signal sequence

B) Which problem occurs and how could it be solved?

C) The packet length is unchanged and node C has the highest priority. Modify the waiting times so that all nodes have send data after nine clock cycles (use table 10.2). The waiting times should be as short as possible. Fill in the signal sequence of the bus nodes, resulting from the modified waiting times (use Figure 10.2). Mark waiting times and collisions that occur, label which graph should be evaluated with a cross.



Node	Packet length	Waiting time
A	1	
B	2	
C	3	

Table 10.2: Modified waiting time

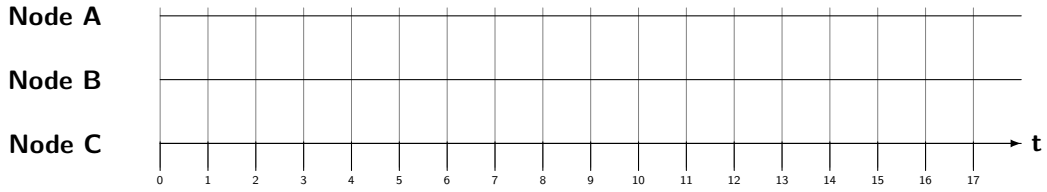


Figure 10.2: Signal sequence

Task 10.2: CSMA/CA

A communication system comprises five communication nodes that use CSMA/CA as arbitration scheme. In order to transmit data a node transmits a dominant start bit (‚0‘) for synchronization purpose. After that a 5 bit message identifier followed and 10 bits of payload data is sent. The message identifiers are unique for each node and all data is sent MSB first. The bus has to cover a maximum distance of $500m$.

A) Name two advantages and two disadvantages of CSMA/CA.

B) Which requirements have to be fulfilled in order to guaranty a faultless function of the system? What are the implications for the transmission rate?

C) Calculate the maximum payload data rate of this bus. Assume a propagation time of $0.66c$ ($c = 3 \cdot 10^8 \frac{m}{s}$).

D) Figure 10.3 shows a timing diagram for the bus system described above. Indicate the identifiers of the given nodes as far as possible (use Table 10.3). Mark undetermined identifiers bits as X!

Node	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4
A					
B					
C					
D					

Table 10.3: Identifiers of the nodes

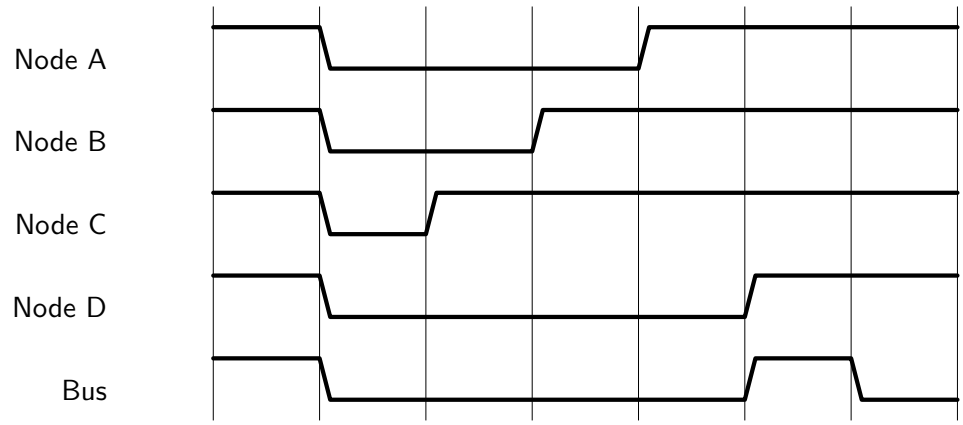


Figure 10.3: Bus Access

E) Which node is granted exclusive access to the bus?

Task 11: Spreading Codes

A) Table 11.1 shows the functions of several sender nodes. Show that these functions fulfill the requirements and can be used to transmit data using CDMA.

Sender node	Function
A	$(+1, +1, -1, -1, +1, +1, -1, -1)$
B	$(+1, +1, +1, +1, -1, +1, -1, +1)$
C	$(+1, +1, -1, -1, -1, -1, +1, +1)$

Table 11.1: Functions for sender nodes

B) An additional node D should also be able to send data at the same time. Find another function for node D and show that your function is valid.

C) Table 11.2 shows the walsh code for a system with four different senders. Only three instead of four senders want to send data. Calculate the resulting signal on the media.

Sender node	Function	Data
A	$(+1, +1, +1, +1)$	"0"
B	$(+1, -1, +1, -1)$	"1"
C	$(+1, +1, -1, -1)$	"1"
D	$(+1, -1, -1, +1)$	-

Table 11.2: Walshcode for four sender nodes

D) Calculate the bit value that the receiver will detect for node D.

E) Assume there is not an analog signal on the media, but a positive and negative value. Calculate the bit value that the receiver will detect for node A and node D. Hint: Think about the tolerance band, when reducing the bandwith of the signal

F) Is it useful to send only two different values instead of the analog signal? Justify your answer!

Task 12: Arbitration

A) A system using centralized daisy-chaining is shown in figure 12.1. An exemplary arbitration cycle of the system is shown in figure 12.2. Assign the correct signals of figure 12.1 to the signals shown in the diagram below (figure 1.2). Justify your choice of assignment with a few sentences. What node is sending data at which point in time? Complete the diagram (figure 12.2) accordingly.

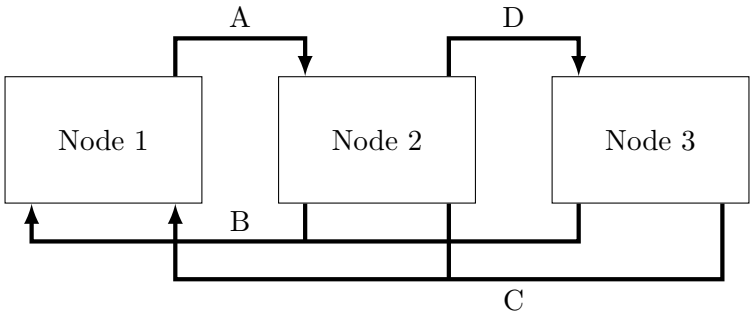


Figure 12.1: Centralized Daisy-chain

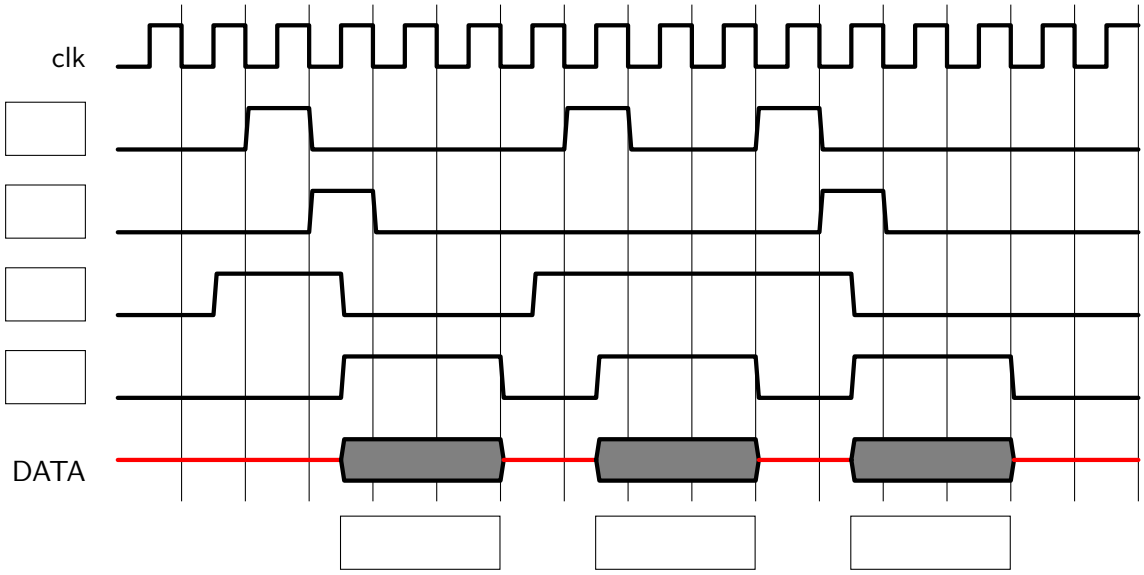


Figure 12.2: Signal flow for Daisy-chain

B) In the decentralized Daisy-chain shown in figure 12.3 a scheduling should be done. The different nodes will set a request at the times given in table 12.1. Only after successful transmission the nodes will remove their request. The sending of the data always needs exactly one time step. This includes token passing and the time needed for the arbitration. Complete Table 12.2 according to the specified arbitration scheme.

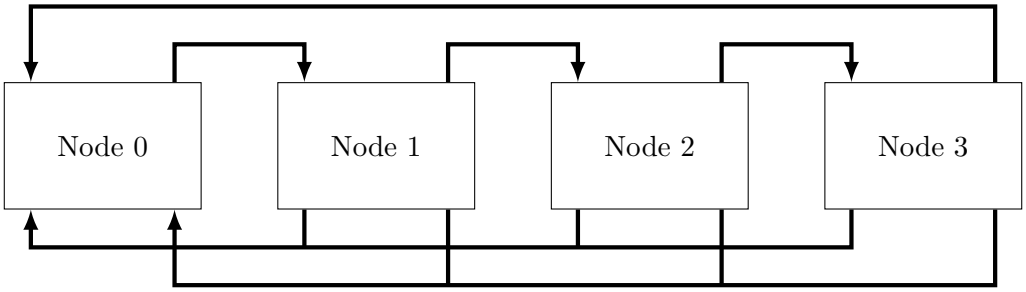


Figure 12.3: Decentralized Daisy-chain

time	Nodes that assert a sending request signal
t_1	Node 2 and Node 3
t_2	Node 1
t_3	Node 0
t_4	Node 0 and Node 1

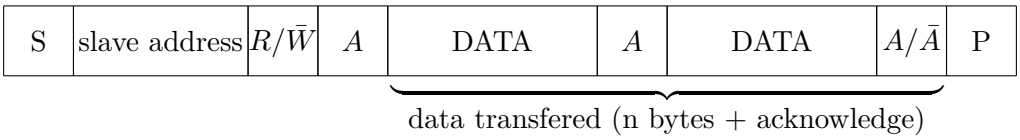
Table 12.1: Time of sending nodes

time	Sending Node
t_0	Node 0
t_1	
t_2	
t_3	
t_4	
t_5	
t_6	

Table 12.2: Solution of Daisy-chain scheduling

Task 13: I²C-Bus Arbitration

The frame format of I²C-bus is shown in figure 13.1. Three master nodes are simultaneously trying to transmit one byte of data to different slaves over the I²C-bus.



term	descripion
S	start condition
slave address	7-bit slave address
$R/\bar{W}$	read/write: read 1, write 0
A	acknowledge from slave
$\bar{A}$	not acknowledge
DATA	8-bit data
P	stop Condition

Figure 13.1: I²C-bus frame format

A) The addresses of the slaves and the data to be send to them is shown in the table 13.1. Complete the signal diagram in the figure 13.2.
Hint: A slave always answers with a positive Acknowledge (0). Which node is winning the arbitration?

node	slave address	data
Master 1	0100110	00011010
Master 2	0100101	10100111
Master 3	0100101	00101101

Table 13.1: test

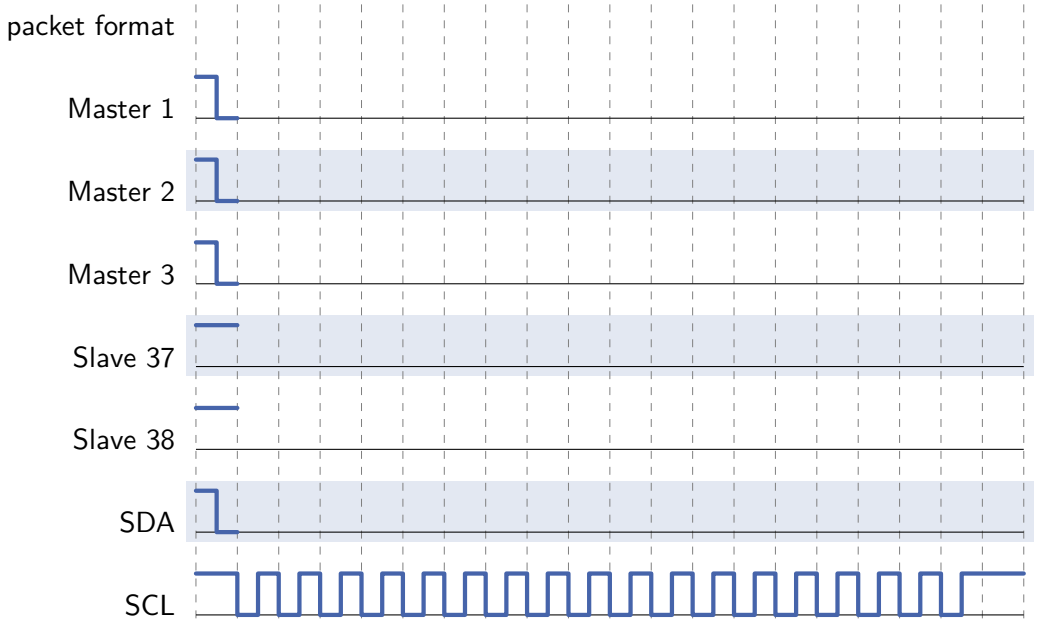


Figure 13.2: Signal sequence

Task 14: Cyclic Redundancy Check

Task 14.1: Transmission

To protect a data transmission, CRC with the generator polynomial $g(x) = x^2 + 1$ is used.

A) Determine the bit string that is associated with the generator polynomial.

B) What is the length of the checksum that is to be appended to the data stream?

C) Calculate the data stream that will be transmitted if the following bit string is to be protected: 1001010101.

Task 14.2: Reception

In a transmission system that uses CRC for error protection, a sender transmits the following bit stream: 100101010110. Due to interferences during transmission the last 4 bits of the bit stream are flipped before reaching the receiving node.

A) Denote the bit stream as it arrives at the receiving node.

B) Carry out the CRC error detection scheme of the receiver assuming that the generator polynomial $g(x) = x2 + 1$ has been used.
What does the receiver conclude from the result? Explain and discuss the reasons for the receiver's conclusion.

Task 14.3: Hardware implementation

A) To protect data transmissions in a mobile device, the CRC scheme is to be implemented using linear feedback registers with XOR operations. Draw the simplified hardware layout for the polynomial CRC-12 ($x^{12} + x^{11} + x^3 + x^2 + x + 1$).

Task 15: I²C-Bus Synchronization

Three I²C Bus Masters want to send data to one slave. Each node needs one time step to read in data from external signal lines (SCL, SDA). The reaction time within each node is neglectably small (0 time steps). The individual masters want to establish a clock signal according to the following table 15.1:

Master	Low period	High period
A	8	4
B	4	12
C	12	8

Table 15.1: clock signals

Assume that Master B is initiating the communication cycle.

A) In general, which functionality does the I²C bus provide for the case that multiple master nodes want to communicate at the same time with the same slave node?

B) Complete the waveforms of the signals that result from the interaction between the nodes on the SCL signal.

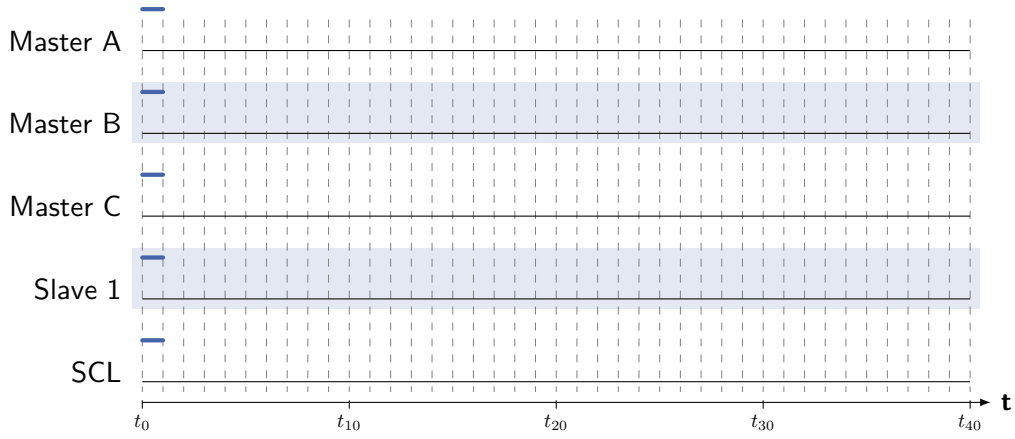


Figure 15.1: Signal sequence

C) In general, which functionality does the I2C bus provide for the case when there is a fast and a slow master node?

Task 16: Actuator Sensor Interface (ASI)

In the following a data transmission on the ASI bus is considered. Thereby a master wants to transmit the bit vector 01001 to the slave having address 26_d. The telegram format of the ASI bus is shown in Figure 16.1.

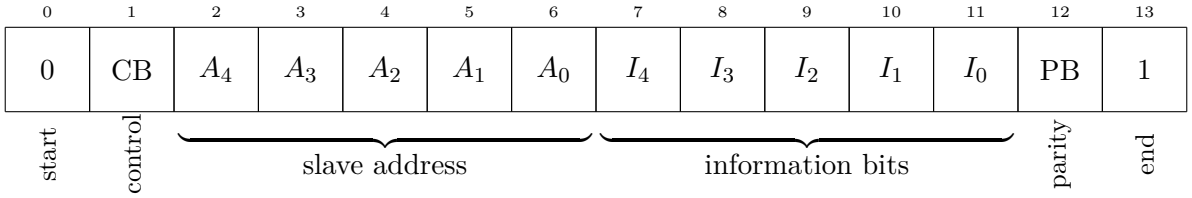


Figure 16.1: ASI packet format, master call

A) Specify the course of the sender voltage on the ASI bus. A time offset does not need to be considered (Note: The control bit must have value '0' for data transmission, use even parity without considering start / stop bits). Use figure 16.2 and Manchester as per IEEE 802.3

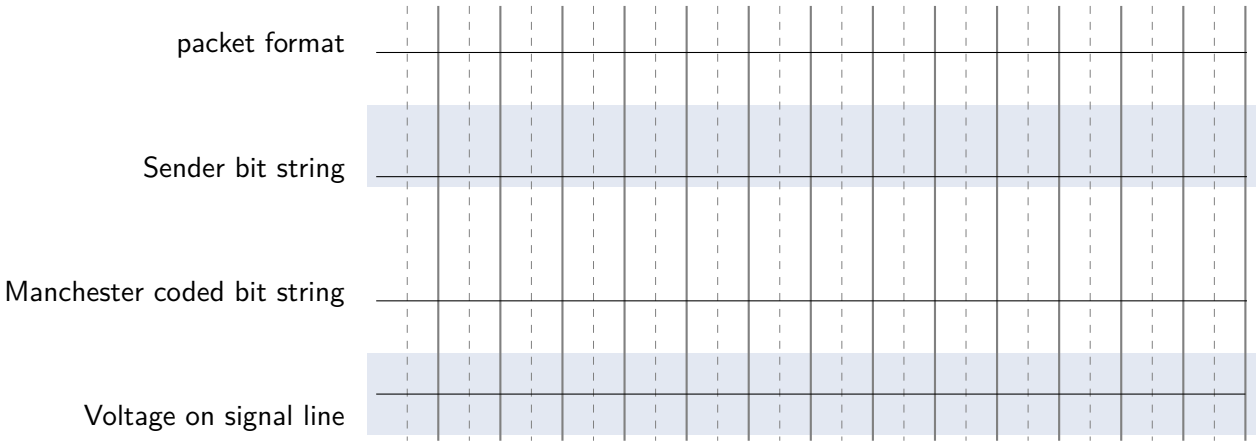


Figure 16.2: Waveform of the sender voltage

B) Figure 16.3 shows the waveform on the ASI bus when transmitting a master call. Due to external influences the transmission has been disturbed. Mark the errors and name the rule(s) by which they are detected.

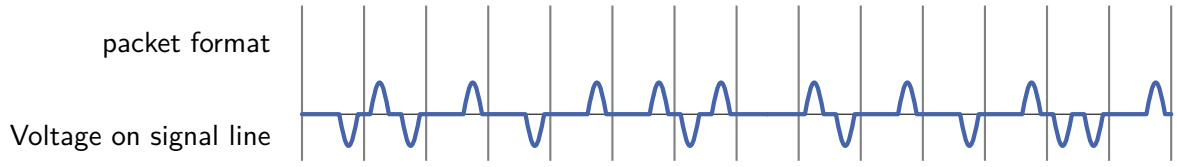


Figure 16.3: Waveform of the sender voltage

Task 17: CAN Bus

Since CAN uses CSMA/CA as arbitration scheme every participant compares the actual bus level with the signal transmitted by itself. Because of that it is important for every participant to be able to evaluate the actual state on the bus before begin of a new bit. Here beside the signal runtime on the bus also the required processing time of the participant itself plays a role.

As given in Figure 17.1, this includes the processing time t_{CAN} of the CAN controller, the times t_{Rx} and t_{Tx} which are needed inside the transceiver for reception and transmission as well as the runtime t_{Bus} on the bus.

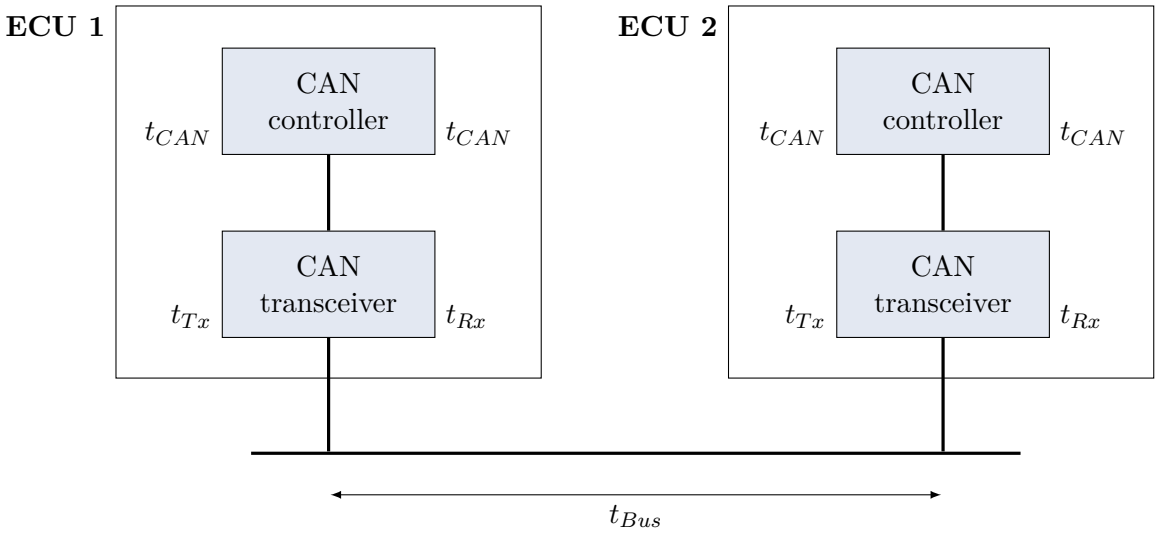


Figure 17.1: CAN bus

A) What is the interrelation between the maximum bus length and the bit transmission rate for CAN? Neglect the processing time inside the ECUs for this question

B) Based on the previous question, specify the maximum bus length for a speed of propagation of $v = 2.3 \cdot 10^8 m/s$ and for the transmission rates of $10 kbit/s$ and $1 Mbit/s$ respectively.

C) Now also consider the delays inside the ECUs. Which data transmission rate can be set as a maximum if the bus length between the two controllers that have furthest distance amounts to 300 meters? The detection of the bus state shall be accomplished after 80 percent of the bit time at latest (assume: $t_{CAN} = 75 nsec$, $t_{Rx} = t_{Tx} = 25 nsec$, $v_{Bus} = 0,2 m/nsec$).

Task 18: PCI bus circle

Figure 18.1 shows the process of reading four data words within a burst on the PCI bus. The signals marked with "*" use negative logic. The FRAME* signal indicates the beginning and the end of a burst transaction. AD is the time multiplexed address- and data-bus. IRDY* (master) und TRDY* (slave) are used to insert waiting cycles after the transmission of an address. A waiting cycle is always inserted when at least one of the two signals is deactivated, that means it shows a high voltage level. All bus participants evaluate the state of a signal line at the rising edge of the clock. The clock frequency is 33.33MHz.

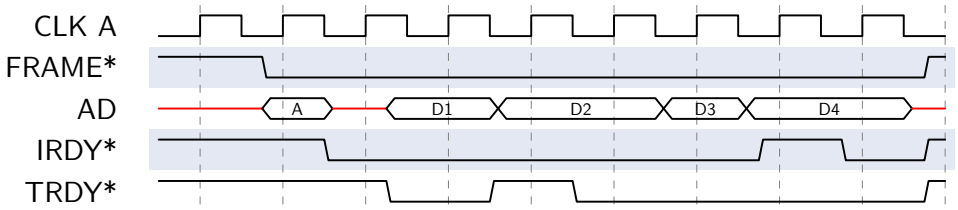


Figure 18.1: Simple PCI burst

A) How many waiting cycles are generated during the read burst given in Figure 18.1?

B) How long is the latency from the point in time when the activation of the FRAME* signal is detected by all bus participants to the point when the first data word can be read?

C) Assume that the address phase of a burst of infinite length has just ended and none of the involved participants forces waiting cycles. What is the data transfer rate of the PCI bus in this ideal case? (Approximation: $1MB = 10^6 Bytes$)

D) The time behavior of the PCI bus that can be seen in the picture is characteristic for a certain category of busses. What is the name of this category?

Task 19: Dijkstra

In Figure 19.1 you can see a network of six nodes (A..F). The nodes each have a different number of ports, numbered from #1 to #4. Each connection between the tiles is annotated with the communication cost. Your task is to generate the routing tables for the individual nodes.

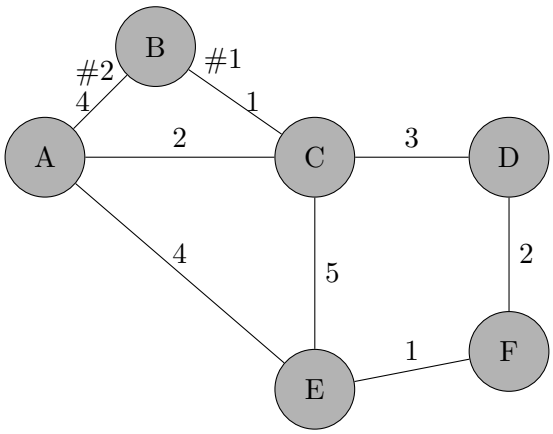


Figure 19.1: Given network topology

A) Determine the shortest path from node B to all other nodes using the Dijkstra-Algorithm. Make use of the tables 19.1 and 19.2.

B) Use the results from the previous task to generate the routing table of node B.

node	step 1 **B**		step 2		step 3		step 4		step 5	
vertex	dist.	pred.	dist.	pred.	dist.	pred.	dist.	pred.	dist.	pred.
A										
B										
C										
D										
E										
F										

Table 19.1: Dijkstra algorithm

node	step 6		step 7	
vertex	dist.	pred.	dist.	pred.
A				
B				
C				
D				
E				
F				

Table 19.2: Dijkstra algorithm

Task 20: Serial Interface

In the figure 20.1 the pulse diagram of a RS232 interface is given. Different transmission frames have been used for the communication. A transmission frame is composed of a start bit ('0'), 5-8 data bits, no (N, none) or one bit for even (E, even) or odd (O, odd) parity, as well as 1 or 2 stop bits (,1'). Possible frame formats are [5..8][N,O,E][1,2], for example 8N1 for 8 data bits, no parity bit and at least 1 stop bit.

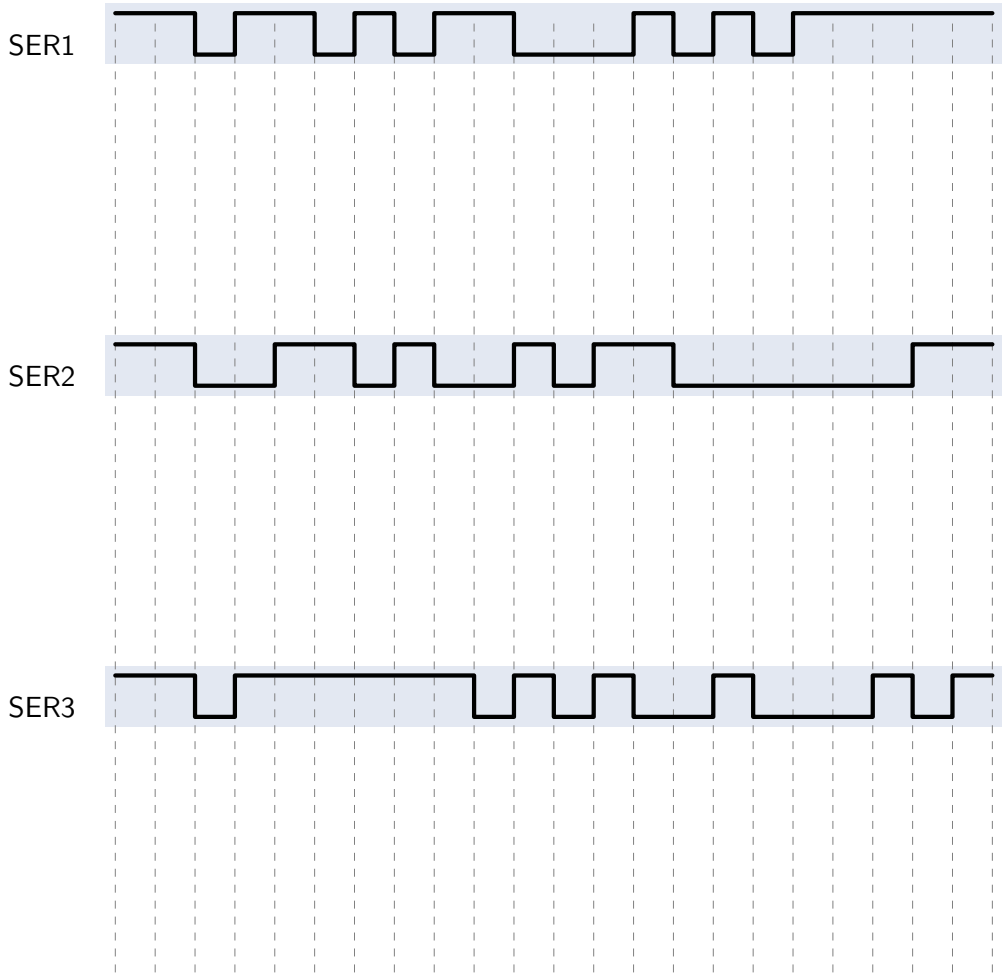


Figure 20.1: Serial interface pulse diagram

A) Give all possible frame formats for the pulse sequences as shown in figure 20.1. All given pulse sequences are describing a correct transmission. Start of a transmission is always the startbit in the third timestep.

B) In the figure below different pulse sequences for a RS232 interface are given. Derive from the figure and the given frame formats if the transmission was error free. Mark the erroneous parts in the pulse diagrams.

C) Is it possible to detect errors without knowing the frame formats?

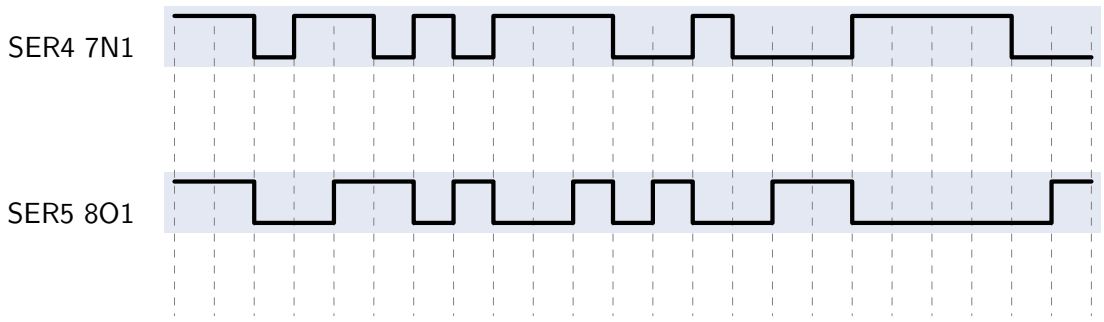


Figure 20.2: RS232 pulse sequences

Task 21: Networks

Task 21.1: General Questions

A) Name three basic building blocks in a Network-on-Chip and explain their function.

B) Which type of switching is preferable in a NoC where the computing units mainly communicate by streaming data, thus in need of high and guaranteed throughput. Justify your decision.

C) What is the edge connectivity and diameter of a 4x4 Torus ?

Task 21.2: Routing

Figure 21.1 shows a 4x4 Mesh network with packet-switching communication.

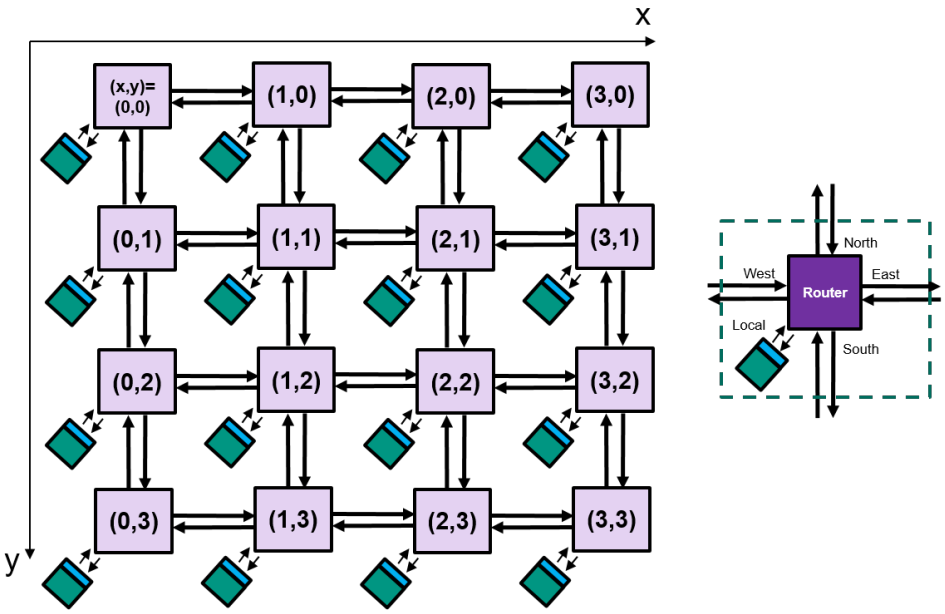


Figure 21.1: 4x4 Mesh network

A) Name all the traversed routers when a packet is sent from $(x, y) = (1, 0)$ to $(3, 3)$ using common XY-Routing. Please provide the coordinates of the traversed router.

B) The routers at address $(1, 0)$ and $(2, 1)$ are experiencing heavy traffic at their east port, such that packets have to wait before being forwarded. To handle such cases a custom routing algorithm called as the "XY-YX" was designed. The "XY-YX" algorithm is described as follows: When a packet arrives, an output port is chosen using the XY routing. If the output port is not busy, the packet is forwarded. If the output port chosen is busy, YX routing is applied to the packet and a new output port is computed. Name all traversed nodes when a packet travels from $(x, y) = (1, 0)$ to $(3, 3)$?

C) Which categories of routing algorithms is the "XY-YX" routing described above associated with? Explain your answer.

D) Now only the east port of router at (1,1) is busy in the network. Using the same "XY-YX" routing described before, name all traversed routers when the source is (0,1) and destination is (3,1). What do you notice ?

E) An additional feature was added to the "XY-YX" algorithm. If the chosen output port is busy even after the YX algorithm was used by the router, then another output port is chosen among the remaining ports according to the priority : North > East > South > West. Now name all traversed routers when the source is (0,1) and destination is (3,1). Again only the east port of router at (1,1) is busy in the network. Is the new routing algorithm minimal ?

F) Now the busy ports are at the south and east of router at (1,1). There is another busy port at south of router (2,0). Use the "XY-YX" routing algorithm with the additional feature mentioned in the above task. Now name all traversed routers when the source is (0,1) and destination is (2,2). What do you notice ?

G) Describe two scenarios: one in which XY Routing is preferable and one in which the "XY-YX" routing is preferable.

Task 22: Quadrature Amplitude Modulation

A) What is the difference between the PSK and the QAM modulation technique?

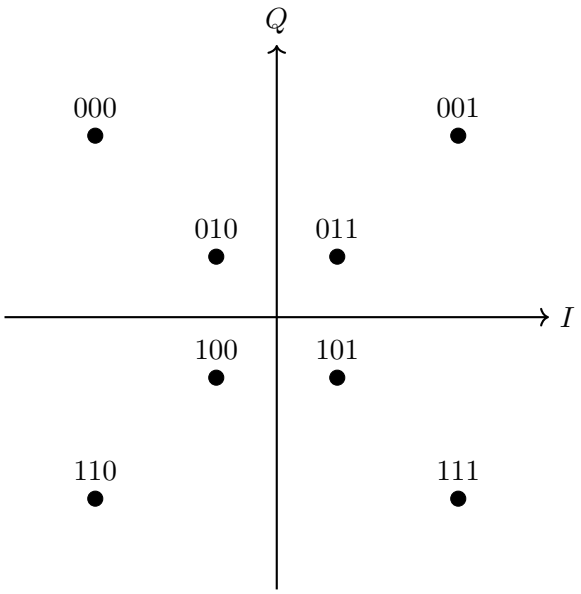


Figure 22.1: Constellation diagram

B) Figure 22.1 shows a constellation diagram for a digital modulation technique. Which type of modulation is used here? Which properties of the signal can be varied with this modulation type?

C) The symbol constellation from Figure 22.1 is now used by a transmitter to modulate data bits on a carrier. The phase φ of the signal is defined relative to a sine reference signal as shown in Figure 22.2. A receiver device now picks up the modulated signal which is plotted in Figure 22.3. Which bits have been transmitted by the sender? Demodulate the signal and write down the resulting bit-stream.

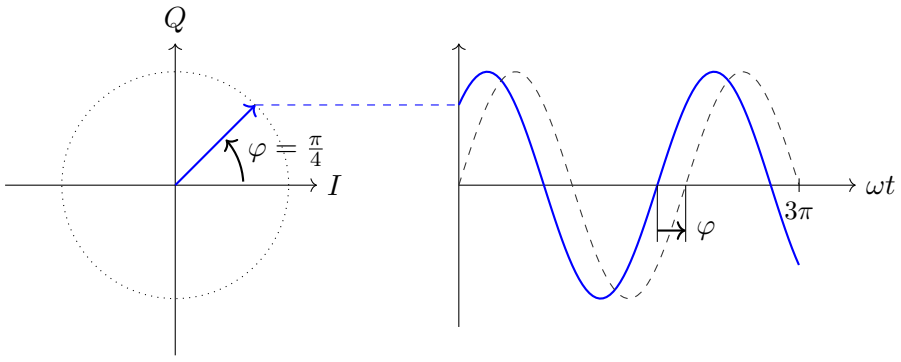


Figure 22.2: Phase difference of a sine signal compared to a reference signal (dashed line $\widehat{=}$ reference signal).

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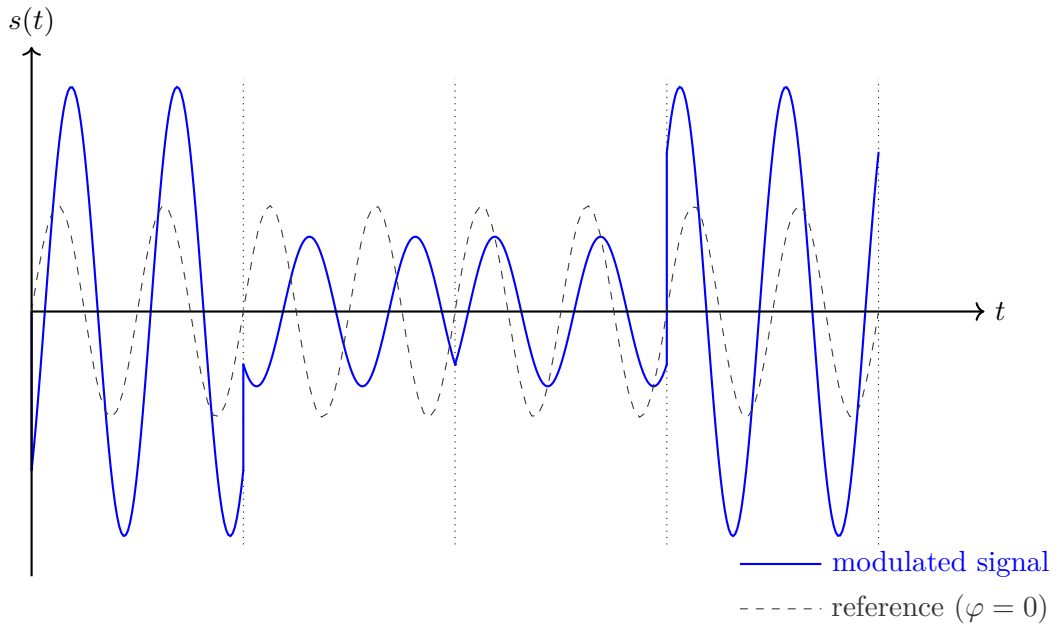

Figure 22.3: A modulated signal which uses the constellation from Figure 22.1 on the preceding page.

D) Now, a signal is modulated with the constellation diagram from Figure 22.4 and transmitted on a coaxial cable. The sender is able to generate a maximum voltage amplitude U_{max} of $\pm\sqrt{72}\,V$. Calculate the acceptance radius r_a for the symbols in the constellation diagram.

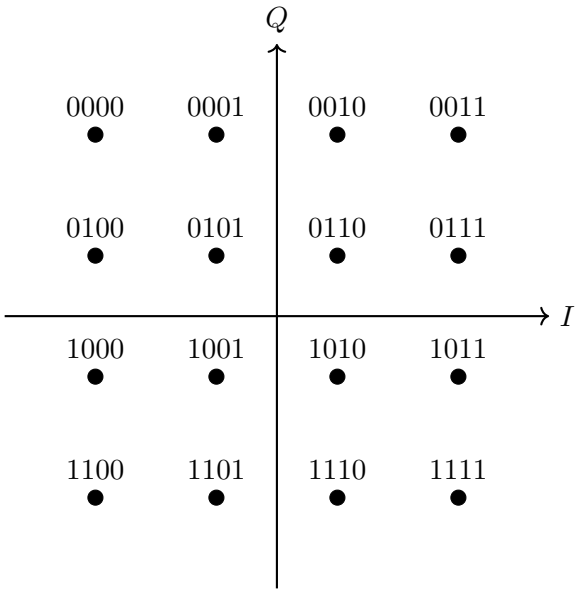

Figure 22.4: Constellation diagram

E) The symbol acceptance radius is a deciding factor for the symbol error probability. However the bit error probability also depends on the encoding of the symbols. The symbol-encoding in Figure 22.4 is not optimal because multiple bits can flip when neighboring symbols are mixed-up due to signal noise. Which kind of encoding could help to solve this problem?

Task 23: Signal Classes

A) The signal in Figure 23.1 is given as the original analog signal. Transform this signal into the other signal classes. Describe for each of the classes how the sampled signal is generated. Use the diagrams in Figure 23.1 to 23.3 with the given sampling points.

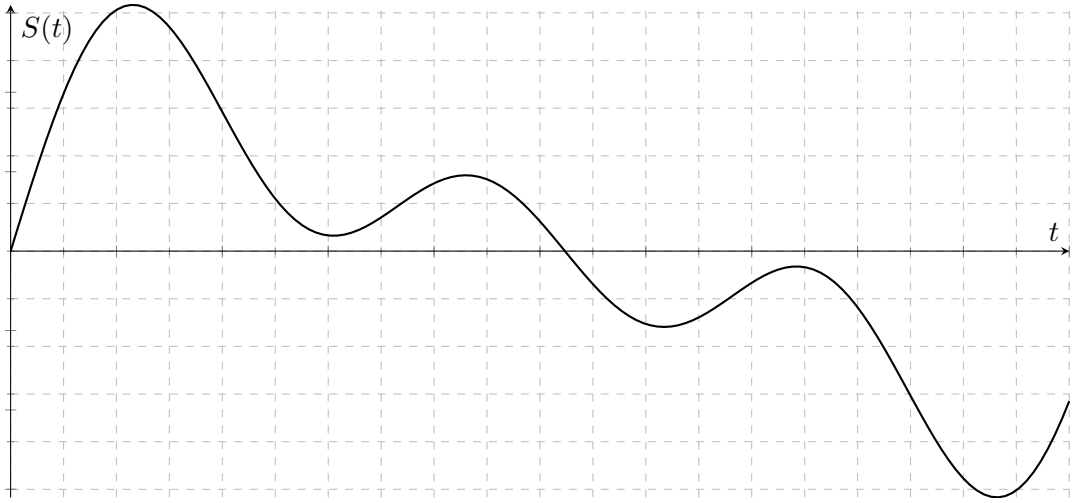

Figure 23.1: signal class:

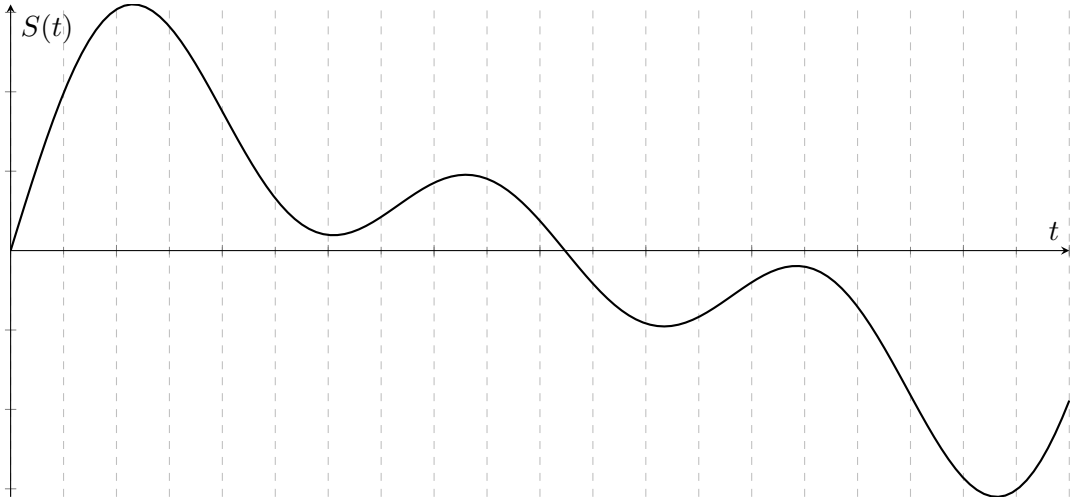

Figure 23.2: signal class:

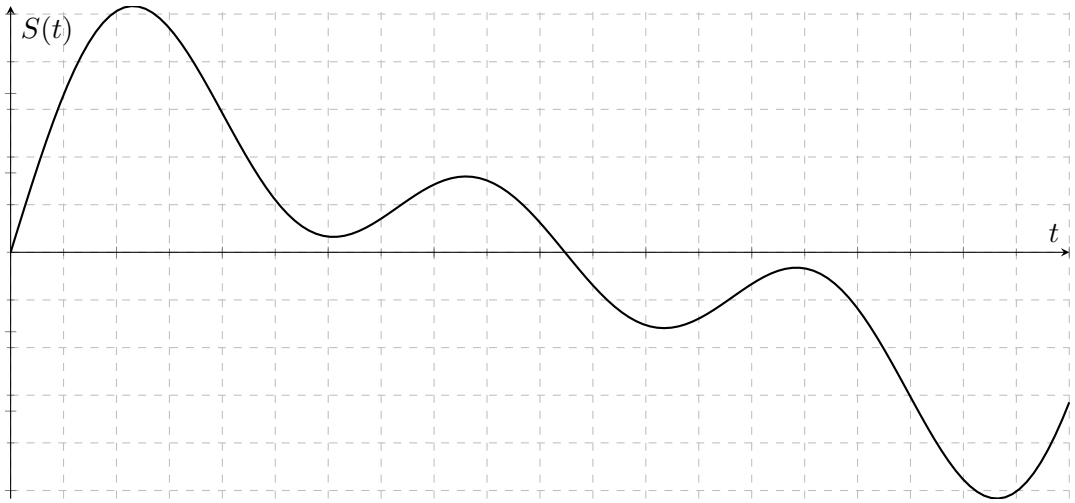

Figure 23.3: signal class:

Task 24: Flow Control

A communication system is given in Figure 24.1. The sender's clock frequency is 1 MHz, the receiver's is 200 kHz. Both partners work synchronously to their own clock signal and try their best to communicate as fast as possible. They apply a Level-triggered Closed-loop Flow Control protocol corresponding to Figure 3.1 for the high-level synchronization.

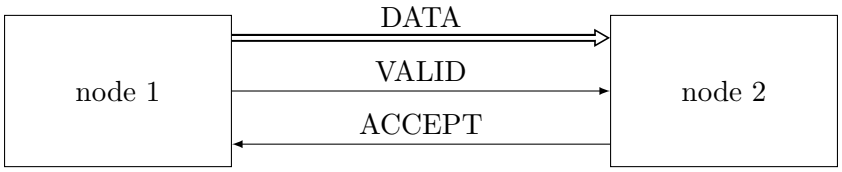

Figure 24.1: Communication system applying Level-triggered Closed-loop Flow Control procedure

A) In Figure 24.2 the sensitive clock edges of the sender and the receiver as well as the signal values for the first sender clock period are shown. In order to avoid violations of setup and hold times, the data is put onto the bus and one clock cycle later the valid signal is set to '1' by the sender. The receiver will also set the accept signal one clock cycle after having received the data. Fill in the progression of all signal lines until the end of the time scale.

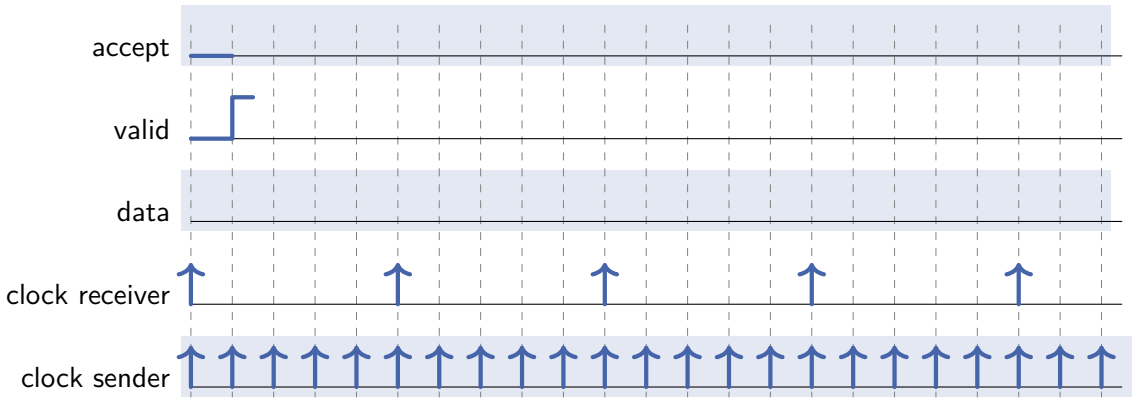

Figure 24.2: Signal progression diagram

B) Is this kind of synchronization free from error in this specific case? Justify your answer.

C) Propose a better solution for this communication scenario.

Task 25: Universal Serial Bus (USB)

A) Consider an USB 1.1 device in reset state. Calculate the current on the bus. Neglect the energy needs of the device itself. Use the circuit in Figure 25.1 as orientation.

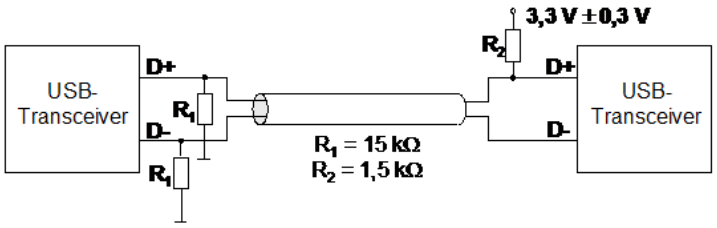

Figure 25.1: Example for resistor configuration at 12Mbit/s

B) To reduce the probability of errors during the handshake phase of a transaction, two data PIDs (DATA0 and DATA1) are used. The data PID is changed after every successful transmission. For that reason the sender and the receiver both have a „data toggle sequence bit“. At the receiver this only changes if correct data with a correct PID has been accepted. At the sender it changes when a valid ACK-Handshake is received. Both participants of a transmission first have to synchronize their bits during the setup phase of a control transfer (see Figure 25.2, the bracketed values correspond to the value of the “data toggle sequence bits”; at X/Y they are still undefined).
Starting from the state of 25.2, specify the flow charts for the following cases (always consider a transfer from host to device):

1. A successful transmission
2. A data packet is rejected and only accepted after being transmitted again
3. The handshake packet of a transmission has been mutilated. The data is transmitted again and accepted then

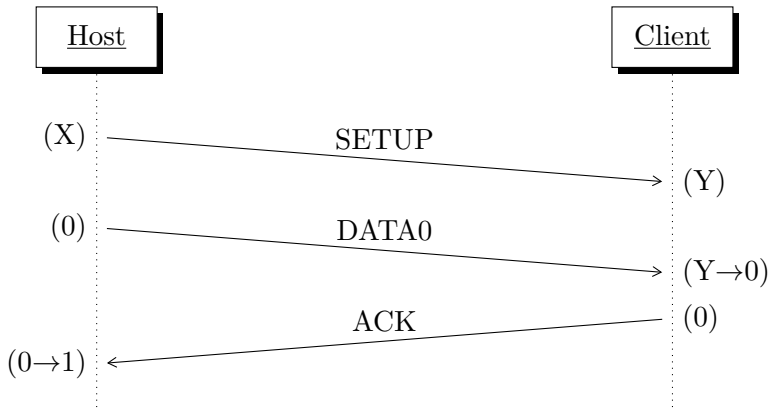

Figure 25.2: Synchronization of the data toggle sequence bits

Task 26: Flexray: Bus Access

In this task we want to investigate the data transmission and scheduling with Flexray. The used topology is shown in Figure 26.1. Additionally, the slot durations for the scheduling are given in Table 26.1.

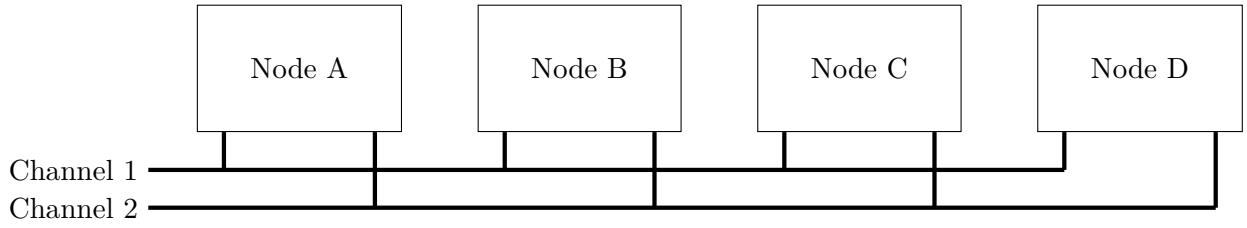

Figure 26.1: Flexray Topology

Static slots	Minislots
$5\mu s$	$100ns$

Table 26.1: Slot durations

A) In Table 26.2 the nodes shown in Figure 26.1 and the assignment of their available frames to the static slots are given. Complete the signal diagram in the Figure 26.2 and perform the static scheduling of the frames according to the Table 26.2.

Node	Static Slots	Frames	Redundant Frames
A	1, 3, 5	A1, A2, A3	A2
B	2, 4	B1, B2	B2
C	1, 4	C1, C2	—
D	5	D1	—

Table 26.2: Static Node Assignments

B) Calculate the duration of a complete communication cycle! Assume a Network Idle Time (NIT) of $1\mu s$ and that all minislots depicted in Figure 26.2 are idle!

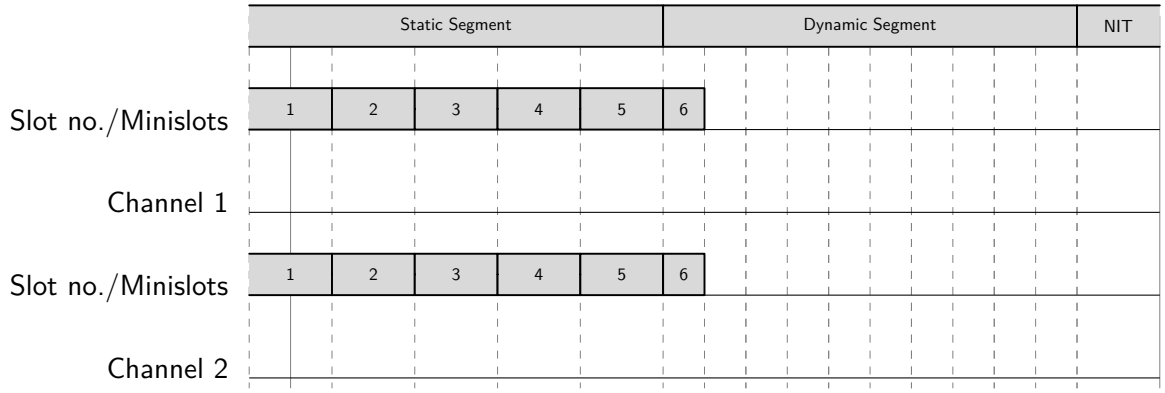

Figure 26.2: Signal sequence

C) What is the purpose of the minislots with regard to bus access, which are used in the dynamic segment of the communication cycle? Is it possible that multiple nodes can own the same minislot? Justify your answer!

D) In Table 26.3 the parameters for the dynamic segment are given. Complete the signal diagram in the Figure 26.2 and perform the dynamic scheduling of the frames for Channel 1 and Channel 2 according to the Table 26.3. Number the minislots with slot IDs dependent on the length of your scheduled frames. Note that each channel offer its own minislots for transmission.

Node	Frames	Slot-ID	Frame Duration
A	A7	7	$100ns$
B	B9	9	$300ns$
C	C8	8	$500ns$
D	D6	6	$400ns$
	D11	11	$200ns$

Table 26.3: Dynamic Segment Parameters